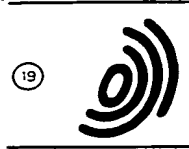


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Improvements in to ATM signal processors.

An ATM signal processor system for processing ATM data cells which in combination define a data package wherein the last cell of a package is characterised by an identifying code, comprising means for multiplexing the cells of different data packages thereby to provide a serial data stream, a server, a buffer store via which the server is fed with the serial data stream, the buffer store having a threshold capacity beyond which cells are discarded, and dis-

carded cell identifier/rejecter means which serves to identify and store the identity of a data package with which a discarded cell is associated, so as to be set thereafter to reject subsequently received cells with the same data package identity, until being reset consequent upon receipt of the last cell of the said package as indicated by its characteristic identifying code.

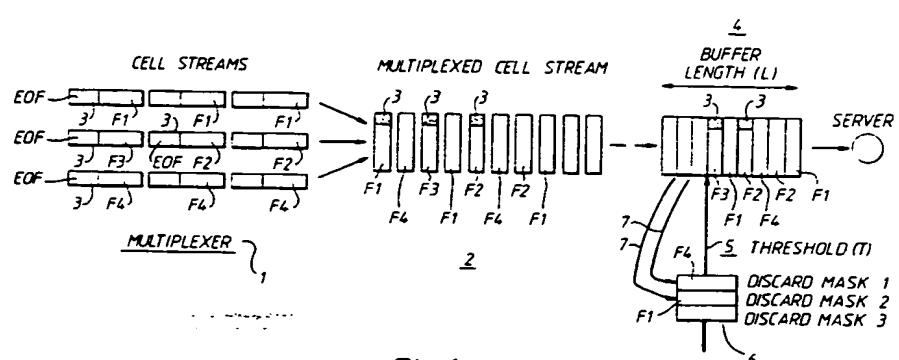


Fig.1

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This invention relates to asynchronous transfer mode (ATM) signal processor systems and more especially it relates to such systems for ATM data transmission, wherein the transmission comprises a number of cells which are transmitted successively and which in combination define a data package or frame wherein the last cell of the package is characterised by an identifying data code.

When a plurality of transmissions are made each relating to a different data package, the cells of the various transmissions are multiplexed or interleaved to provide a serial data stream. It will be appreciated that ATM data traffic is inherently bursty in nature and in order to accommodate widely varying data rates arriving at a server, a serial buffer store is normally provided via which the server is fed with the serial data stream. Since in times of heavy traffic the capacity of the buffer store may be inadequate, the buffer store is arranged to have an in-built threshold capacity beyond which data is discarded and lost whereby retransmission is required.

It will be appreciated that when a cell is discarded, the data package of which it forms a part is corrupted such that subsequently transmitted cells which form part of the same data package are useless. As the buffer store empties however, useless subsequently received cells relating to the corrupted data package may nevertheless be stored in the buffer so as to occupy buffer storage capacity which might be more fruitfully used whereby data transmission efficiency is reduced.

It is an object of the present invention to provide an ATM signal processor system, wherein the cells of data packages corrupted as aforesaid are not needlessly stored whereby system efficiency is improved.

According to the present invention an ATM signal processor system for processing ATM data cells which in combination define a data package wherein the last cell of a package is characterised by an identifying code, comprises means for multiplexing the cells of different data packages thereby to provide a serial data stream, a server, a buffer store via which the server is fed with the serial data stream, the buffer store having a threshold capacity beyond which cells are discarded, and discarded cell identifier/rejecter means which serves to identify and store the identity of a data package with which a discarded cell is associated, so as to be set thereafter to reject subsequently received cells with the same data package identity, until being reset consequent upon receipt of the last cell of the said package as indicated by its characteristic identifying code.

The discarded cell identifier/rejecter may comprise address register means in which the address of discarded cells is stored and inhibitor means

responsive to the address of subsequently received cells for deleting them if their address corresponds to an address in the said register, an address being deleted from the register, consequent upon reception of a cell having that address, and additionally being identified as a last cell in a data package by its characteristic identifying code.

The address register means may comprise a mask register.

One embodiment of the invention will now be described by way of example only with reference to the accompanying drawing.

Referring now to the drawing, cell streams relating to data packages F1, F2, F3 and F4 are fed through a multiplexer 1 to provide a serial data stream 2. Each data package may comprise a number of cells, the final cell only of which is identified as such by a characteristic code final cell 3 as shown schematically in the drawing.

The multiplexed serial cell stream is fed to a buffer 4 including a threshold capacity 5 beyond which cells are discarded. The addresses of discarded cells are stored in a discard mask store register 6 which comprises a plurality of mask address stores for storing addresses appertaining to a number of different cells. When the address of a discarded cell has been stored, subsequently received cells are examined and details of their address are fed over the lines 7 to the discard mask store register 6 and if correspondence obtains between the address of an incoming cell and an address stored therein, that incoming cell is deleted. In the event that a cell arrives having an address which corresponds to one of the addresses stored in the register 6 and additionally is identified by a characteristic code as a last cell 3 of a data package then the discard mask address store appertaining thereto is emptied so as to be available to receive the address of a newly discarded cell.

It will be appreciated that once a cell has been deleted due to buffer overflow, when the threshold has been reached, (which is the most common cause of cell loss), the rest of the cells which form part of the same frame or data package will also be deleted without increasing frame loss, whereby optimum use of the buffer store for wanted cells is facilitated. Thus by deleting all cells making up a particular frame in conditions of high buffer usage, the continuing deletion of specific cells making up a frame even after the buffer usage has dropped below threshold T, will reduce the chance of other frames being deleted.

Various modifications may be made to the arrangements shown without departing from the scope of the invention and for example any suitable address identifying/storage/discard means may be used as will be well known to those skilled

in the art.

Claims

1. An ATM signal processor system for processing ATM data cells which in combination define a data package wherein the last cell of a package is characterised by an identifying code, comprising means for multiplexing the cells of different data packages thereby to provide a serial data stream, a server, a buffer store via which the server is fed with the serial data stream, the buffer store having a threshold capacity beyond which cells are discarded, and discarded cell identifier/rejecter means which serves to identify and store the identity of a data package with which a discarded cell is associated, so as to be set thereafter to reject subsequently received cells with the same data package identity, until being reset consequent upon receipt of the last cell of the said package as indicated by its characteristic identifying code. 5
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2. A system as claimed in claim 1, wherein the discarded cell identifier/rejecter comprises address register means in which the address of discarded cells is stored and inhibitor means responsive to the address of subsequently received cells for deleting them if their address corresponds to an address in the said register, an address being deleted from the register, consequent upon reception of a cell having that address, and additionally being identified as a last cell in a data package by its characteristic identifying code. 25
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3. A system as claimed in claim 2, wherein the address register means comprises a mask register. 40

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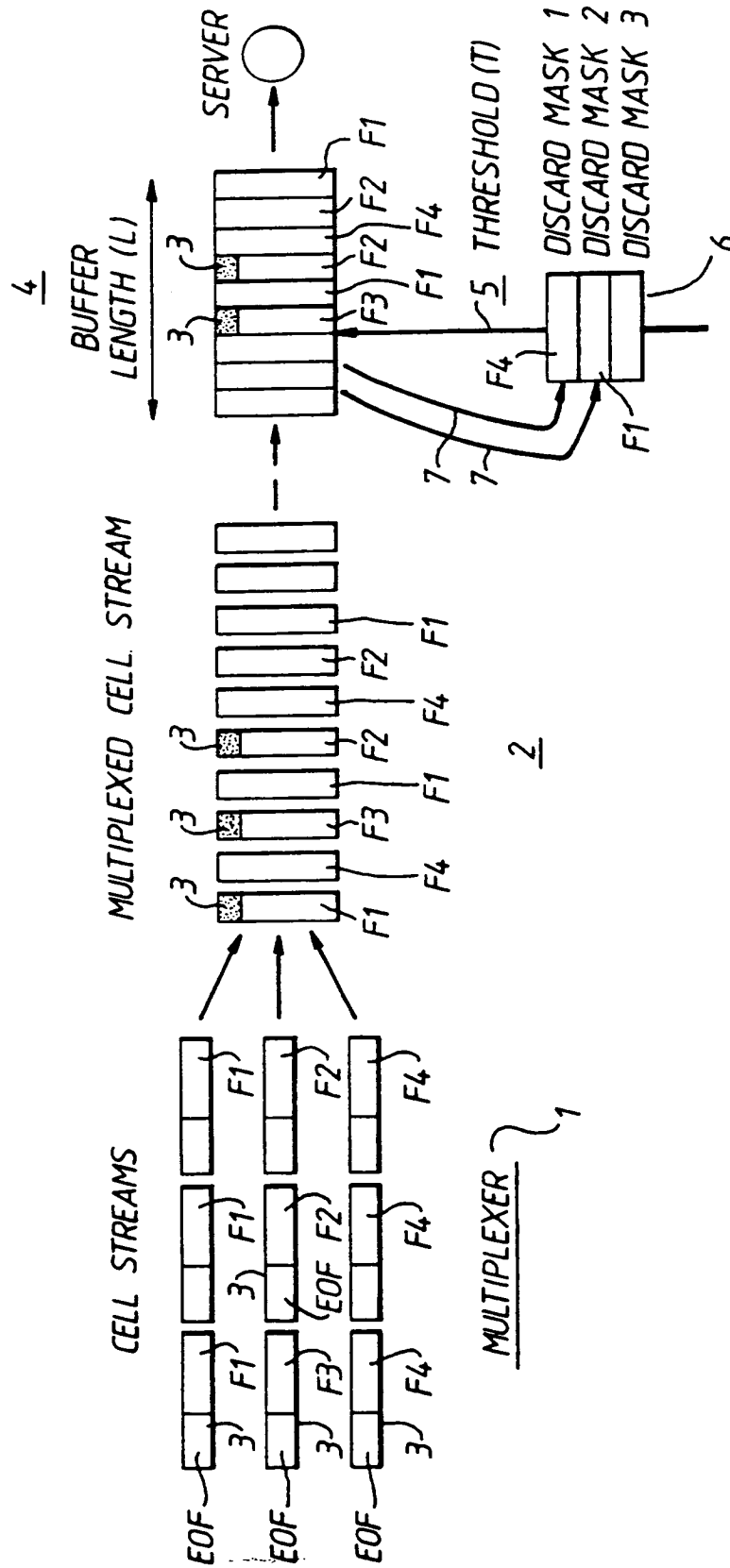


Fig.1

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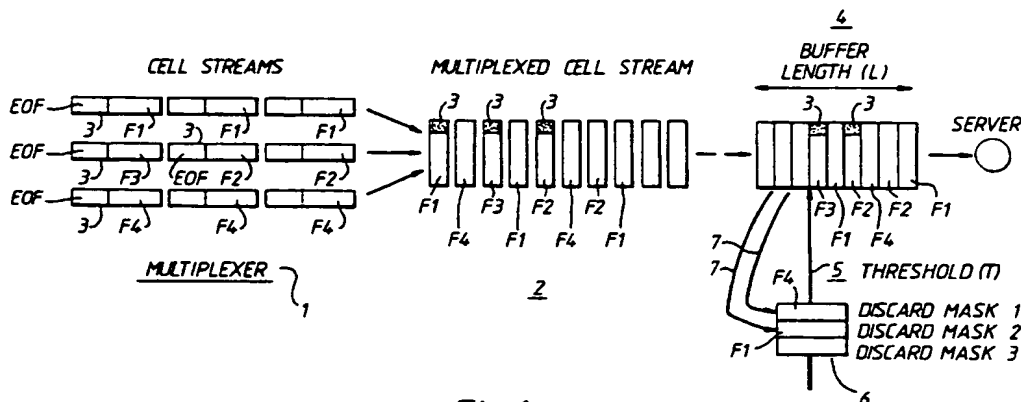
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(54) Improvements in to ATM signal processors

(57) An ATM signal processor system is disclosed for processing ATM data cells which in combination define a data package wherein the last cell of a package is characterised by an identifying code, comprising means for multiplexing the cells of different data packages thereby to provide a serial data stream, a server, a buffer store via which the server is fed with the serial data stream, the buffer store having a threshold capacity beyond which cells are discarded, and discarded cell

identifier/rejecter means which serves to identify and store the identity of a data package with which a discarded cell is associated, so as to be set thereafter to reject subsequently received cells with the same data package identity, until being reset consequent upon receipt of the last cell of the said package as indicated by its characteristic identifying code.



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EUROPEAN SEARCH REPORT

Application Number
EP 93 11 1177

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
X	COOPER C A ET AL: "TOWARD A BROADBAND CONGESTION CONTROL STRATEGY" IEEE NETWORK: THE MAGAZINE OF COMPUTER COMMUNICATIONS, vol. 4, no. 3, May 1990, pages 18-23. XP000160044 * page 18, left-hand column, paragraph 3 *	1	H04L12/56 H04Q11/04
A	* page 19, left-hand column, paragraph 1-3 * * figure 2 * * page 21, right-hand column, paragraph 1-2 *	2.3	
A	TAKEO KOINUMA ET AL: "AN ATM SWITCHING SYSTEM BASED ON A DISTRIBUTED CONTROL ARCHITECTURE" INNOVATIONS IN SWITCHING TECHNOLOGY, STOCKHOLM, MAY 28 - JUNE 1, 1990, vol. 5, 28 May 1990, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, pages 21-26, XP000130921 * sections 4.1, 4.2 and 5 *	1-3	
			TECHNICAL FIELDS SEARCHED (Int.Cl.5)
			H04L H04Q
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 3 March 1998	Examiner Lindner, A
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